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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication number E2456-97000
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For Safety information, Warranties, and Regulatory information, see the pages behind the index

HP E2456A MC68306 Preprocessor Interface

The HP E2456A Preprocessor Interface—At a Glance

The HP E2456A Preprocessor Interface provides a complete interface for state or timing analysis between any Motorola MC68306 target system and the following HP logic analyzers:

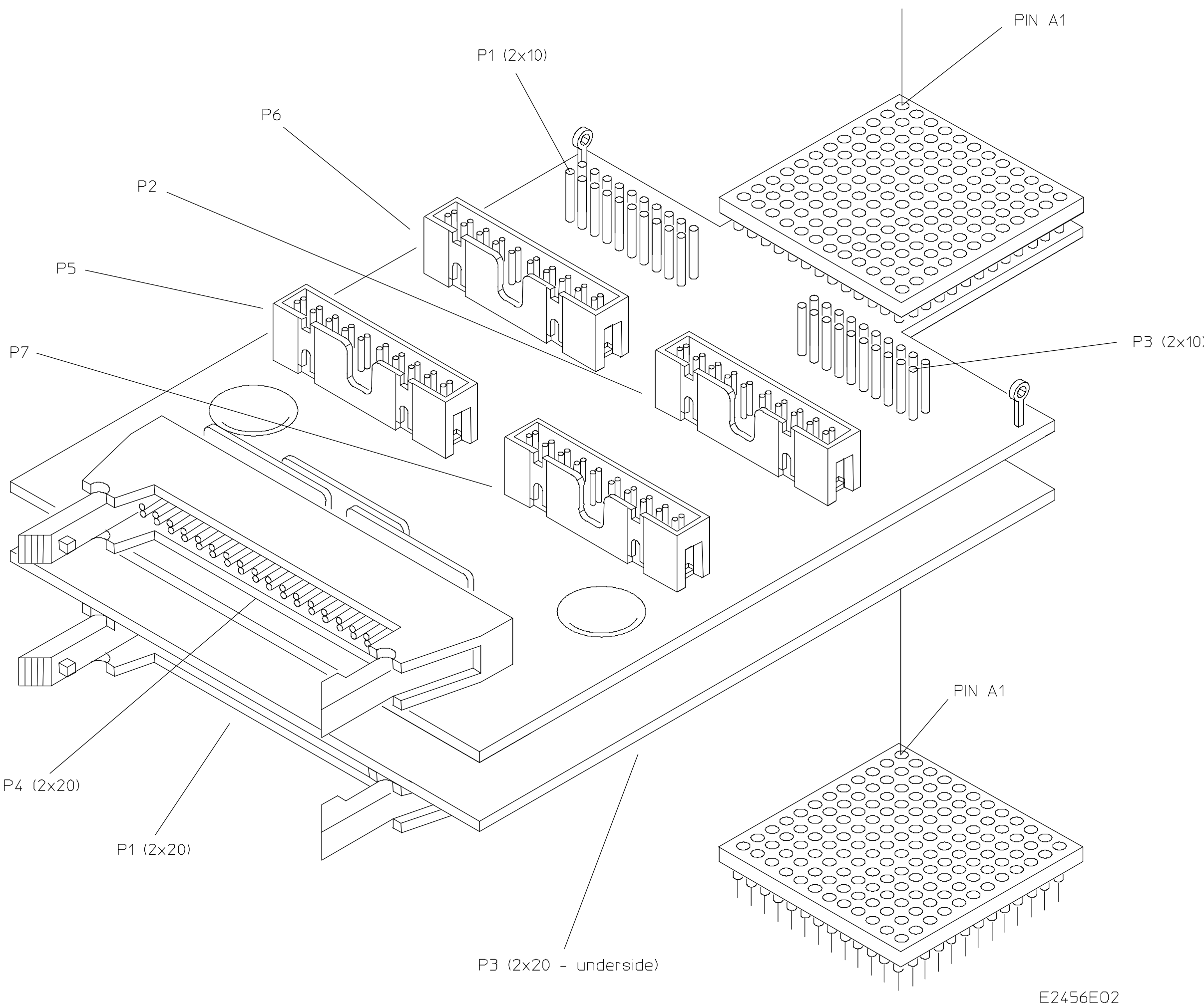
- HP 1650A
- HP 1650B
- HP 1652B
- HP 16510A
- HP 16510B
- HP 16511B
- HP 16550A (one- or two-card)
- HP 16555A (one- or two-card)
- HP 1660A/61A/62A
- HP 1660AS/61AS/62AS (with oscilloscope)

The preprocessor interface connects the target microprocessor to the logic analyzer, and performs any functions unique to the target microprocessor.

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the preprocessor interface. The inverse assembler allows you to obtain displays of the MC68306 data bus in 68000 core assembly language mnemonics.

The HP E2456A Preprocessor Interface requires the HP E3417A 132-pin QFP adapter, which clamps over the existing processor, and supports limited rotation for connecting to target systems with physical layout limitations. The preprocessor connects to the HP E3417A adapter via a 144-pin full matrix PGA socket. The HP E2456A does not support the 144-pin TQFP processor package.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.



HP E2456A Preprocessor Interface

In This Book

This book is the user's guide for the HP E2456A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters and one appendix:

Chapter 1 explains how to install and configure the preprocessor interface for state or timing analysis with the supported logic analyzers.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assembler and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

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Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2456A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.

Before You Begin

This section lists the logic analyzers supported by the HP E2456A, and provides other information about the analyzers and the preprocessor interface.

Equipment Supplied

- The preprocessor interface hardware, which includes the preprocessor circuit card.
- The inverse assembler software and configuration files on a 3.5-inch disk.
- This User's Guide.

Minimum Equipment Required

- The HP E2456A MC68306 preprocessor interface and inverse assembler.
- The HP E3417A 132-pin QFP adapter.
- One of the logic analyzers listed in the following table:

Table 1 **Logic Analyzers Supported**

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
1650A[1]	80	25 MHz	100 MHz	1 k states
1650B	80	35 MHz	100 MHz	1 k states
1652B	80	35 MHz	100 MHz	1 k states
16510A	80	25 MHz	100 MHz	1 k states
16510B	80	35 MHz	100 MHz	1 k states
16511B	160	35 MHz	100 MHz	1 k states
16550A (one card)	102	100 MHz	250 MHz	4 k states
16550A (two card)	204	100 MHz	250 MHz	4 k states
16555A (one card)	68	100 MHz	250 MHz	1 M states
16555A (two card)	136	100 MHz	250 MHz	1 M states
1660A/AS	136	100 MHz	250 MHz	4 k states
1661A/AS	102	100 MHz	250 MHz	4 k states
1662A/AS	68	100 MHz	250 MHz	4 k states

1. The HP 1650A requires system software version V1.11 or higher.

Setting Up the Preprocessor Interface Hardware

Setting up for the preprocessor interface hardware consists of the following major steps:

1 Turn off the logic analyzer and the target system.

Caution

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

3 Install the preprocessor interface in the target system.

4 Connect the logic analyzer pods to the cable connectors of the preprocessor interface board.

The remainder of this section contains a separate subsection for each logic analyzer this interface supports that show the analyzer pod cable connections.

The remainder of this section describes these general steps in more detail.

To select state or timing analysis

The HP E2456A preprocessor interface uses the same connections and configuration for both state and timing analysis. The only difference is that you choose Timing as the Type in the module Configuration menu of your logic analyzer. See "To set up the preprocessor interface for timing" later in this chapter and also Chapter 3 for line loading and timing skew (if any) information.

> The terminated (2X20) P4 connector provides delayed versions of ~UDS and ~LDS. For correct timing information on these signals, use the unterminated (2X10) P7 connector with either a termination adapter (HP 01650-63203) or the General Purpose (GP) probes supplied with your logic analyzer.

To connect to the target system

1. To prevent equipment damage, remove power from both the logic analyzer and the target system.
2. Using the instructions in the "QFP Probe Adapter Assembly Operating Note," connect the probe adapter assembly to the target system microprocessor. Ensure that pin 1 is properly aligned.

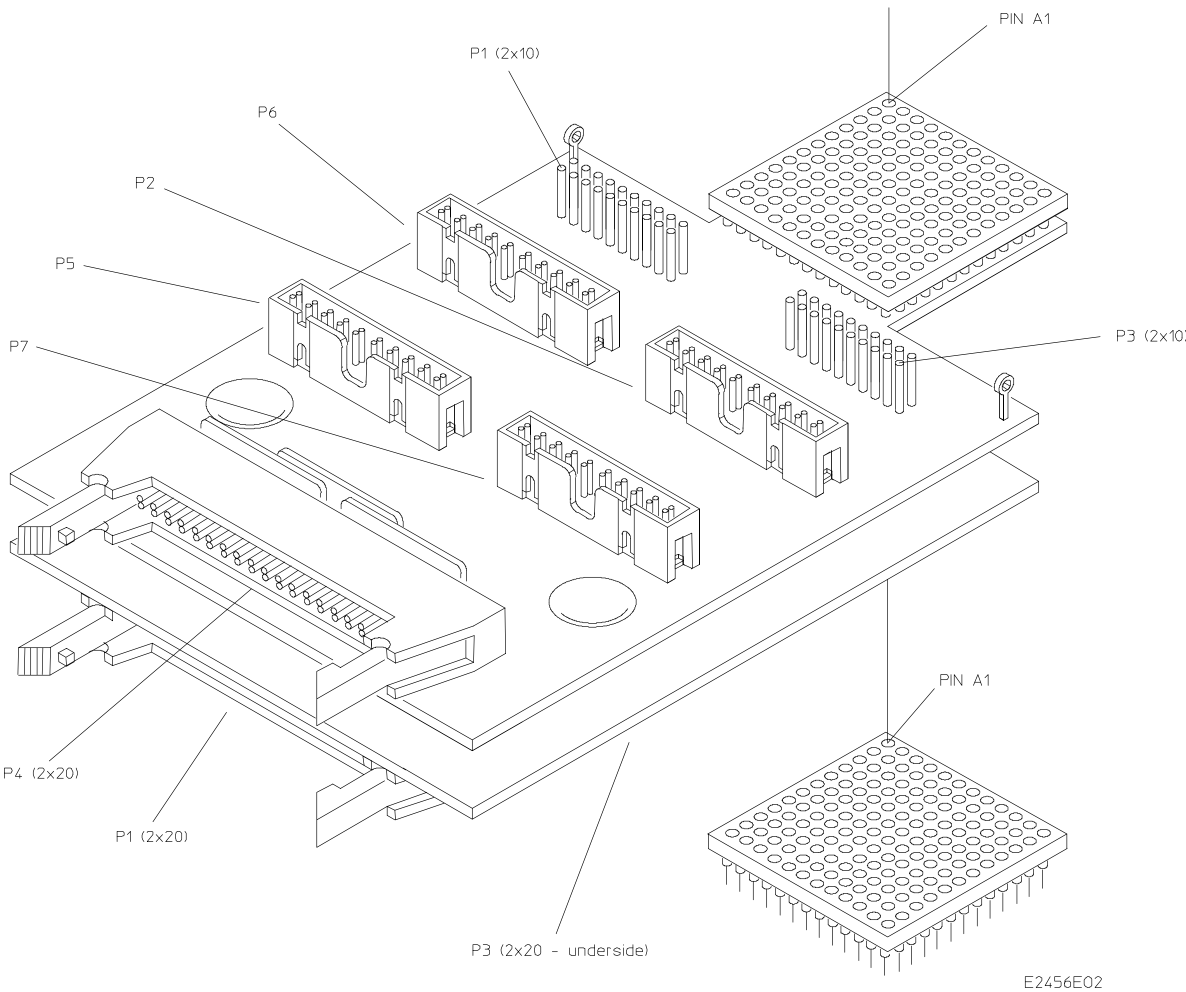
Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 and pin A1 on the preprocessor interface, probe adapter assembly, and microprocessor prior to making any connection. Also, take care to align the preprocessor interface connector with the pins on the probe adapter assembly so that all pins are making contact.

The preprocessor interface requires a QFP Probe Adapter Assembly for connecting to the MC68306 microprocessor. The probe adapter assembly allows the preprocessor interface to be connected without removing the microprocessor from the target system. The adapter supports rotations of 0, 90, 180, and 270 degrees. See the next section for information about rotated connections.

3. Install the preprocessor interface into the PGA socket on the QFP probe adapter, again ensuring that pin A1 is properly aligned.

Figure 1



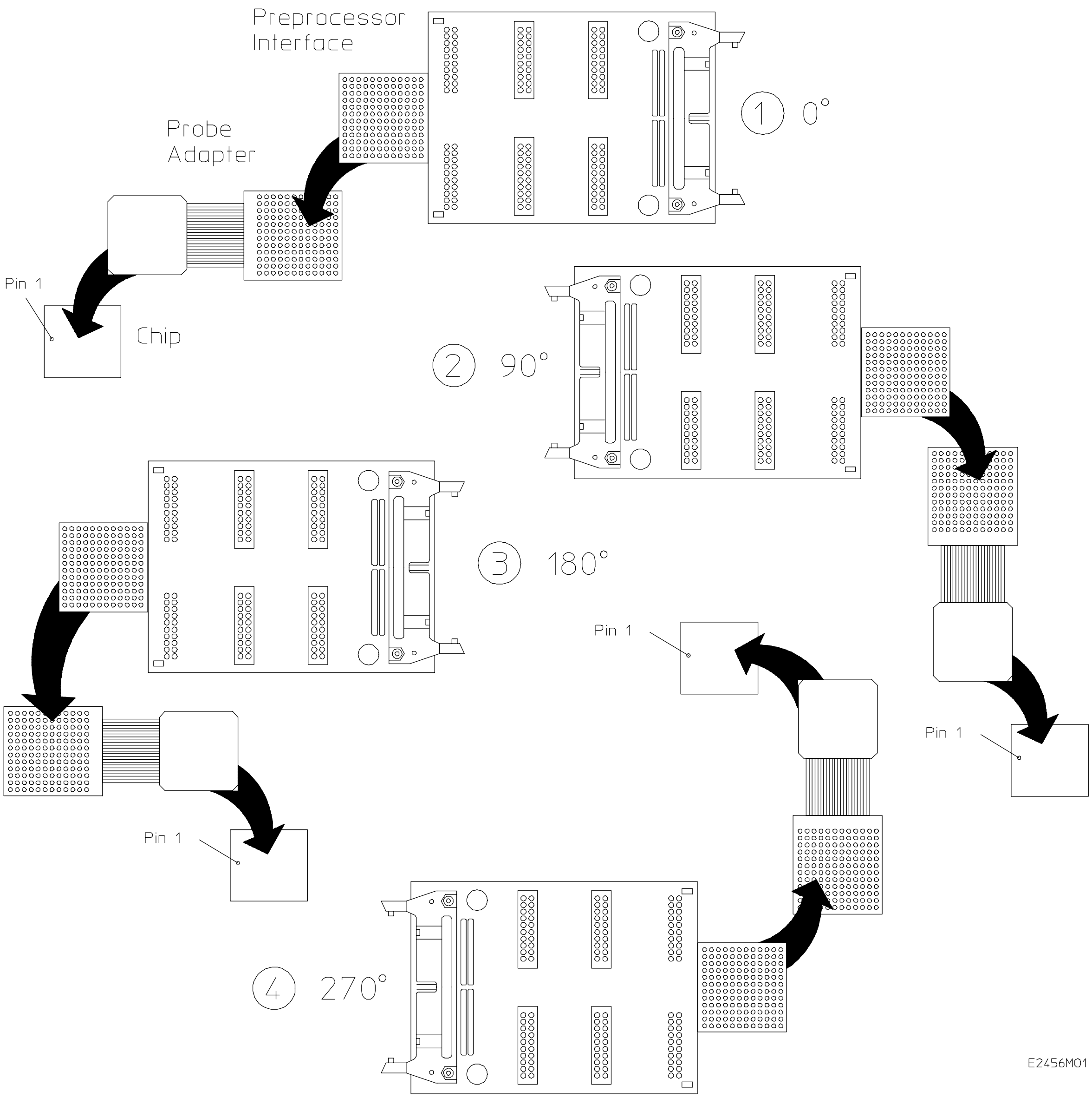
Preprocessor Interface Assembly

To rotate the adapter connection

- **Connect the adapter and preprocessor in one of the rotations shown in Figure 2.**

The HP E3417A adapter supports rotations of 0, 90, 180, and 270 degrees. First, rotate the adapter with respect to the microprocessor the desired number of degrees. Then, rotate the preprocessor with respect to the adapter the same number of degrees. Rotation and perhaps the use of additional PGA pin protector adapters can allow you to clamp onto difficult-to-reach processors.

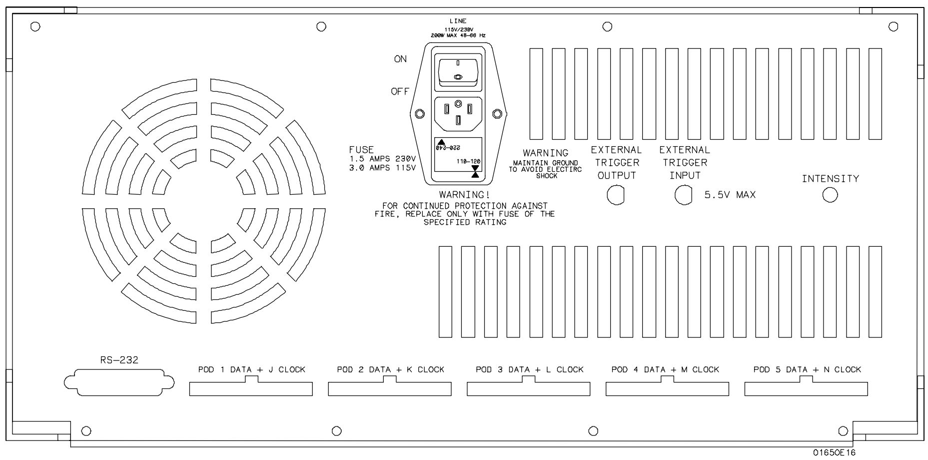
Figure 2



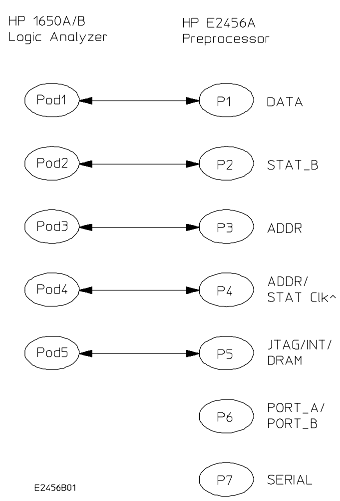
Adapter Rotation Orientations

To connect to the HP 1650A/B analyzer

1. Locate the pod cables in the back of the analyzer.



2. Connect the pod cables to the preprocessor interface according to this diagram.

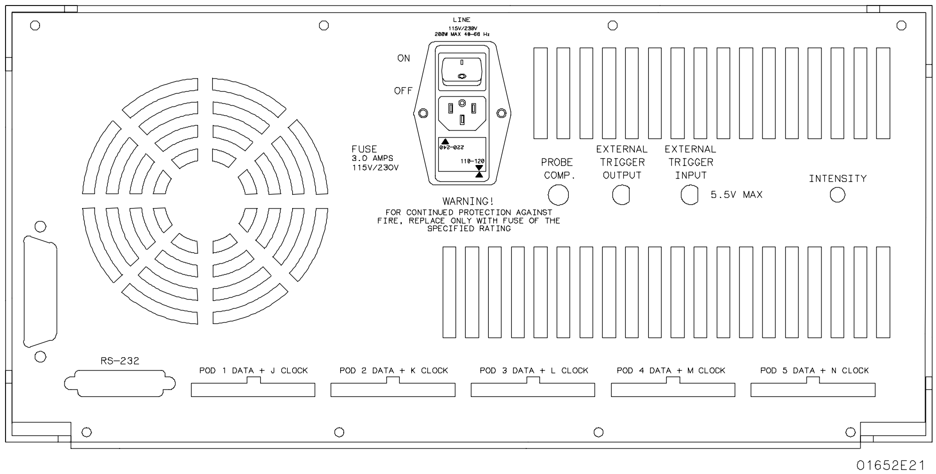


3. Load the configuration file **C68306E0**.

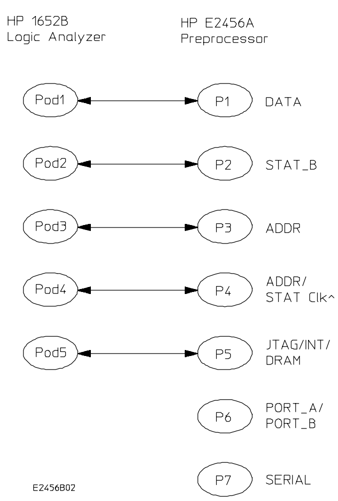
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 1652B analyzer

1. Locate the pod cables in the back of the analyzer.



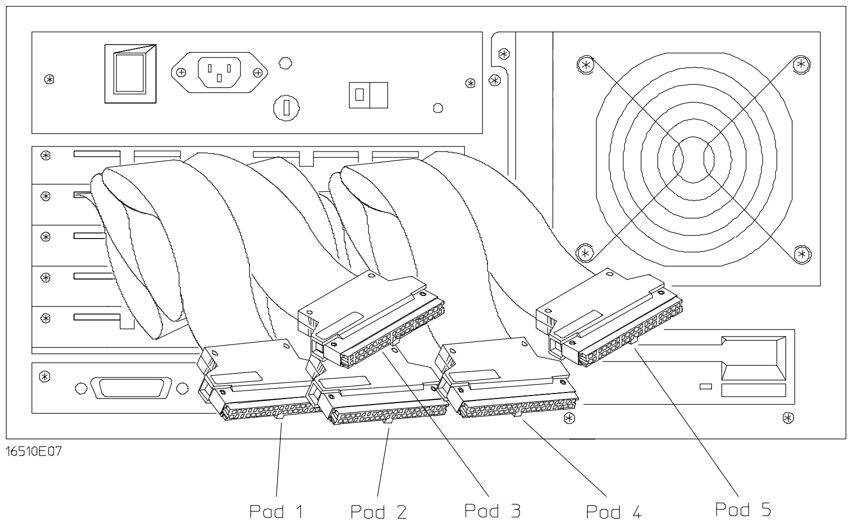
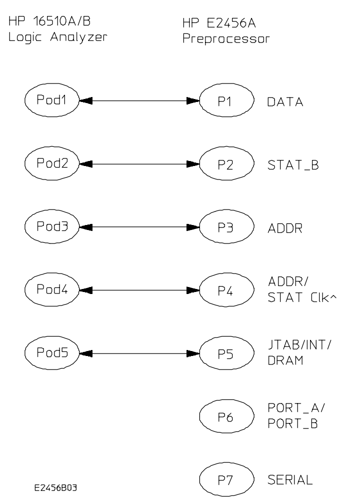
2. Connect the pod cables to the preprocessor interface according to this diagram.



3. Load the configuration file **C68306E0**.

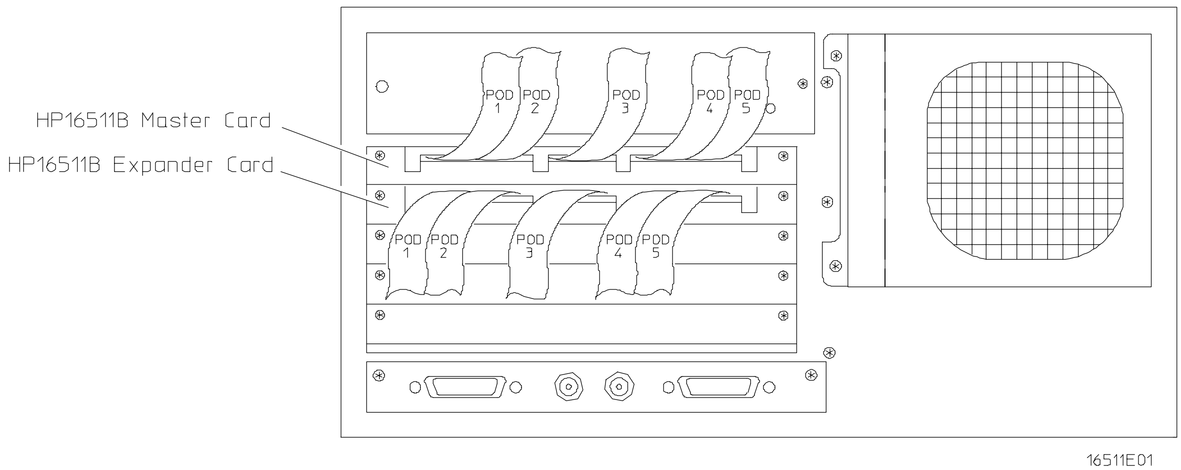
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 16510A/B analyzer

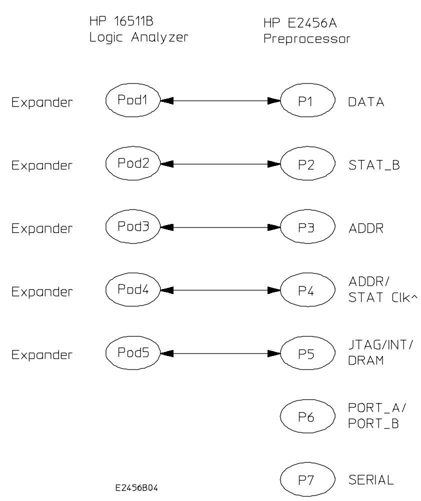
<table>
<tr><td colspan="2">1. Locate the pod cables in the back of the analyzer.</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>2. Connect the pod cables to the preprocessor interface according to this diagram.</td><td>3. Load the configuration file C68306E0.</td></tr>
<tr><td>
</td><td>P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.</td></tr>
</table>

To connect to the HP 16511B analyzer

1. Locate the cards and pod cables in the back of the analyzer (slot positions are relative, actual card positions may vary).



2. Connect the pod cables to the preprocessor interface according to this diagram.

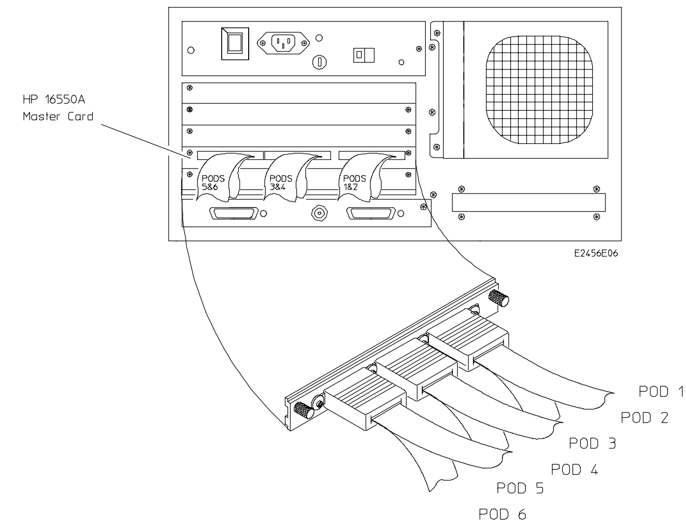


3. Load the configuration file **C68306E2**.

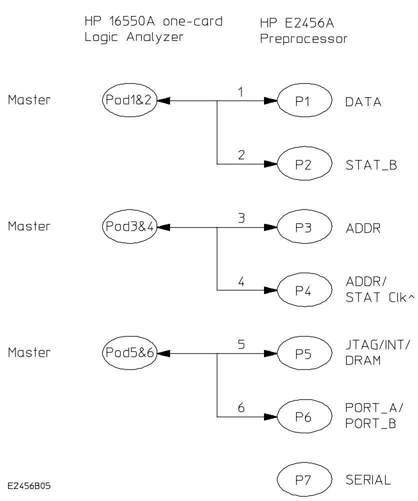
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 16550A one-card analyzer

1. Locate the card and pod cables in the back of the analyzer.



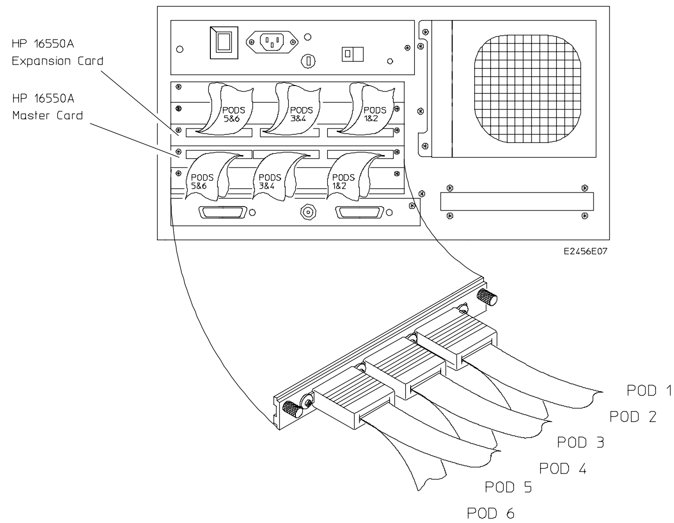
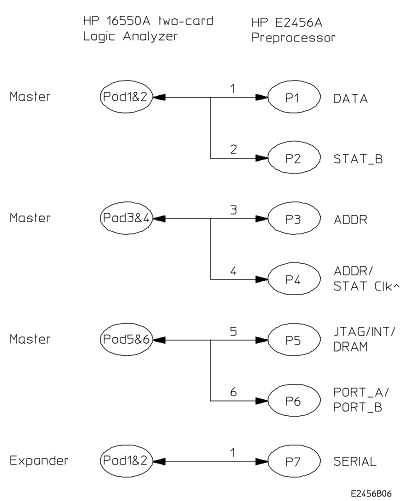
2. Connect the pod cables to the preprocessor interface according to this diagram.



3. Load the configuration file **C68306S1**.

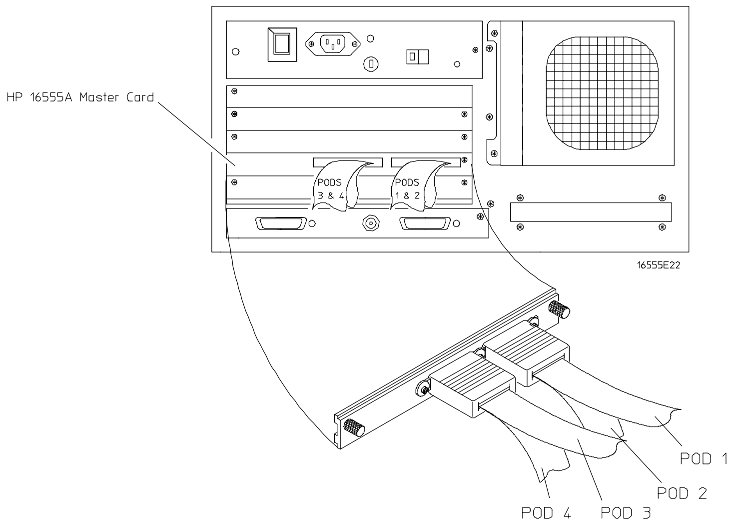
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 16550A two-card analyzer

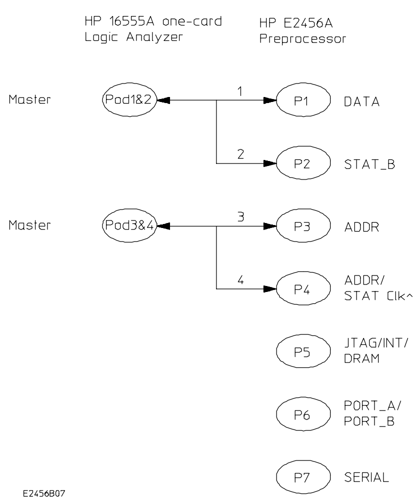
<table>
<tr><td colspan="2">1. Locate the cards and pod cables in the back of the analyzer (slot positions are relative, actual card positions may vary).</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>2. Connect the pod cables to the preprocessor interface according to this diagram.</td><td>3. Load the configuration file C68306S2.</td></tr>
<tr><td>
</td><td>P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.</td></tr>
</table>

To connect to the HP 16555A one-card analyzer

1. Locate the card and pod cables in the back of the analyzer.



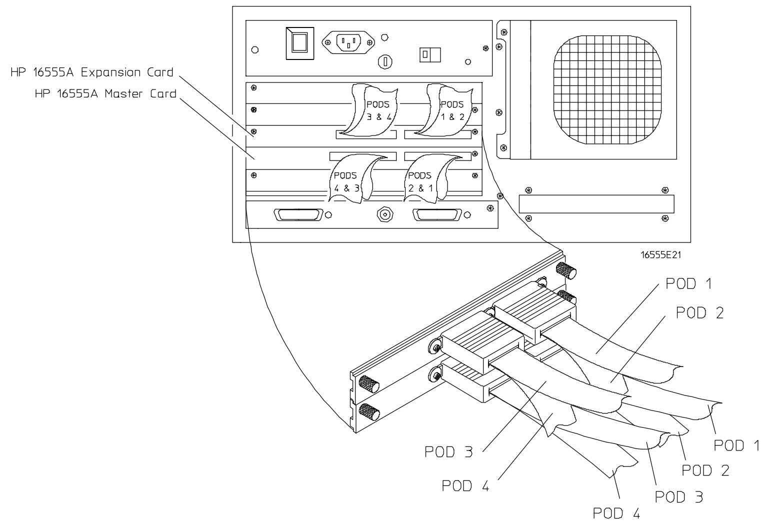
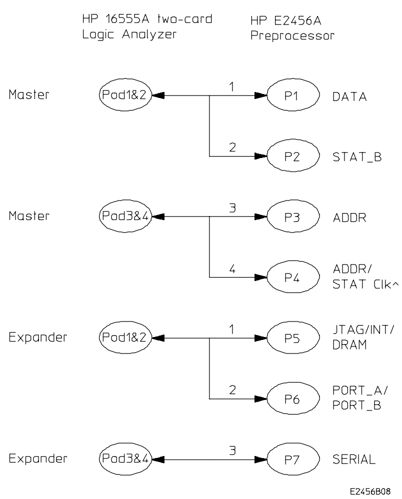
2. Connect the pod cables to the preprocessor interface according to this diagram.



3. Load the configuration file **C68306M1**.

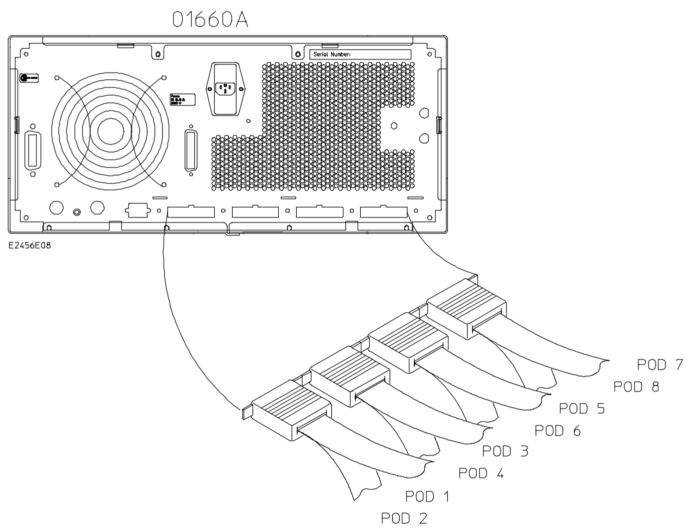
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 16555A two-card analyzer

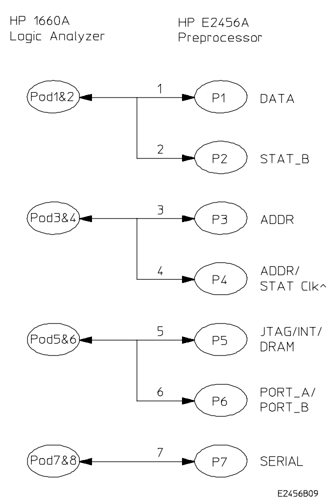
1. Locate the cards and pod cables in the back of the analyzer (slot positions are relative, actual card positions may vary).	
	
2. Connect the pod cables to the preprocessor interface according to this diagram.	**3.** Load the configuration file **C68306M2**.
	P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 1660A/AS analyzer

1. Locate the pod cables in the back of the analyzer.



2. Connect the pod cables to the preprocessor interface according to this diagram.

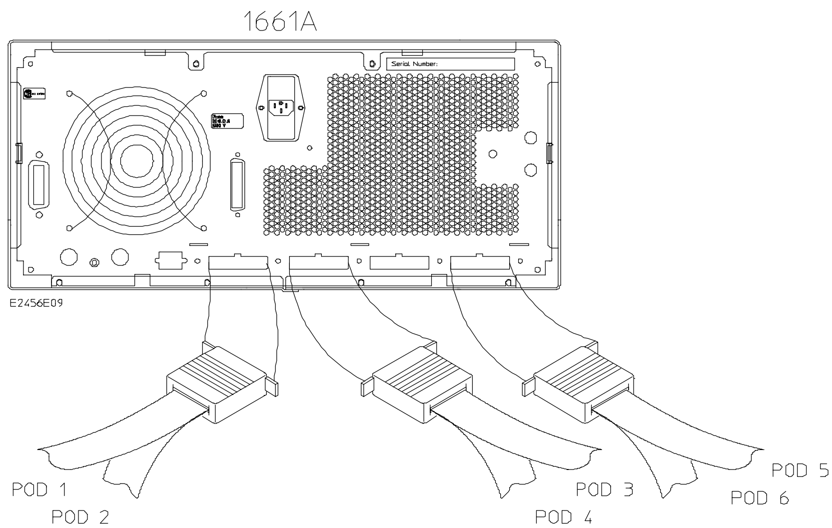


3. Load the configuration file **C68306J0**.

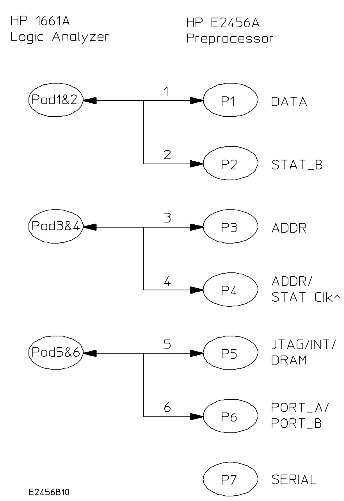
P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 1661A/AS analyzer

1. Locate the pod cables in the back of the analyzer.



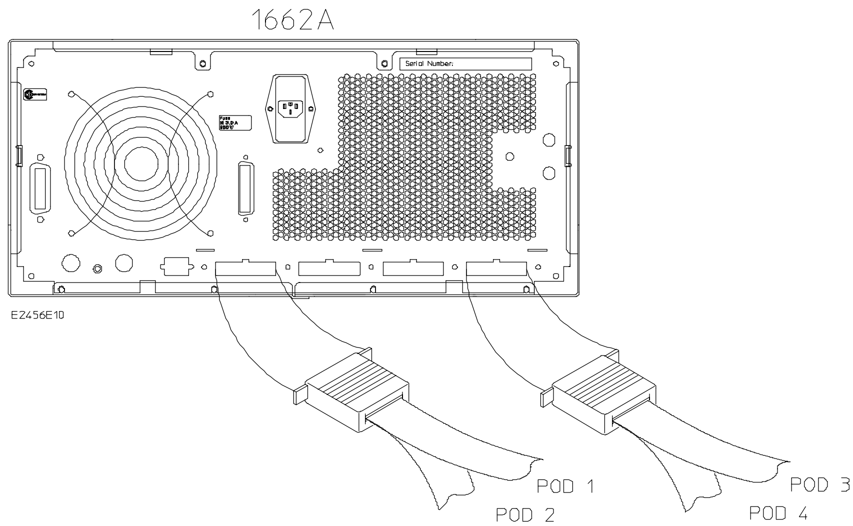
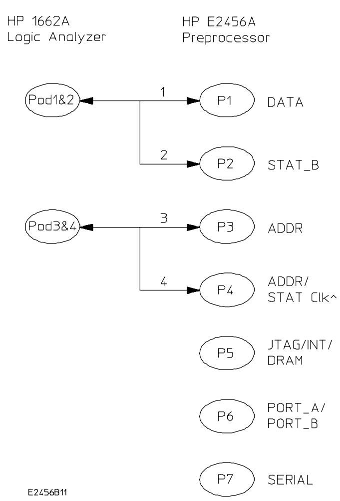
2. Connect the pod cables to the preprocessor interface according to this diagram.



3. Load the configuration file **C68306S1**.

P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.

To connect to the HP 1662A/AS analyzer

<table>
<tr><td colspan="2">1. Locate the pod cables in the back of the analyzer.</td></tr>
<tr><td colspan="2">
</td></tr>
<tr><td>2. Connect the pod cables to the preprocessor interface according to this diagram.</td><td>3. Load the configuration file C68306J2.</td></tr>
<tr><td>
</td><td>P1 and P3 on the preprocessor side refer to the terminated 2X20 connectors, not the unterminated 2X10 connectors.</td></tr>
</table>

To probe the preprocessor interface with an oscilloscope

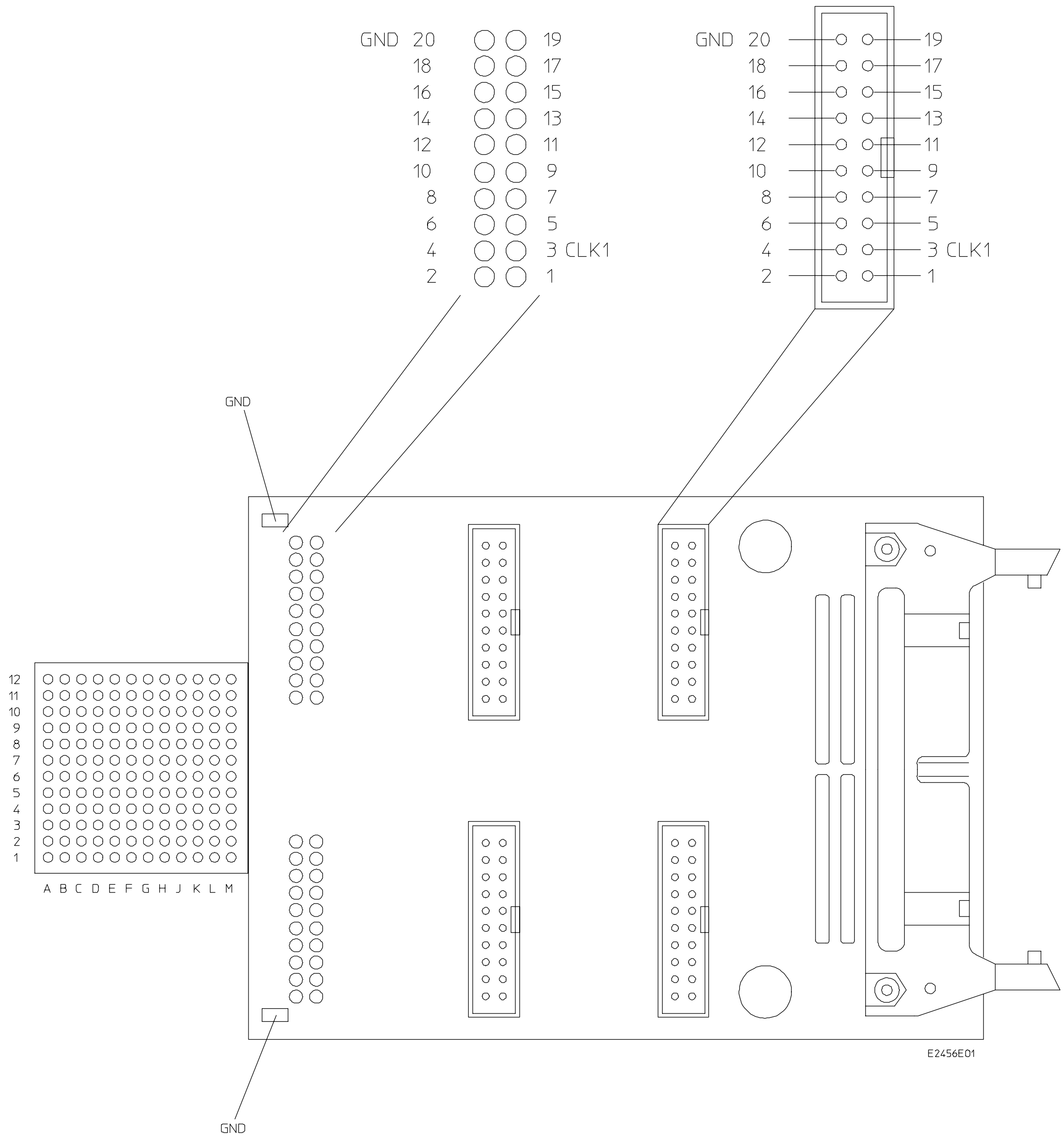
1 **Connect the ground lead of the oscilloscope probe to one of the ground pins on the preprocessor interface.**

There are two ground pins on the top of the preprocessor interface. Refer to Figure 3 for the locations of the ground pins.

2 **Connect the other lead to the signal to be measured.**

You also can probe all microprocessor signals at the PGA socket. Chapter 3 includes an illustration showing the locations of the preprocessor signals on the PGA socket.

Figure 3



Pin Numbers and Ground Pins

To connect the termination adapters

1 Align the key on the male end of the termination adapter with the slot on the connector of one of the logic analyzer cables (not shown), and push the termination adapter into the connector.

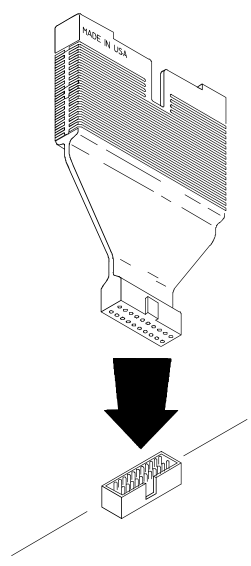
2 Connect the female end of the termination adapter to the preprocessor interface as shown in the figure below. For connectors without a guide slot, orient the adapter the same as for other connectors.

The logic analyzer probes must be terminated for correct operation. On the preprocessor interface, there are nine connectors.

- P4 only has a terminated connector (2x20 pins).
- P2, P5, P6 and P7 only have nonterminated connectors (2x10 pins).
- P1 and P3 have both terminated and nonterminated connectors.

The terminated connectors may be connected directly to the logic analyzer. The nonterminated connectors must be probed by using either the General Purpose probes (shipped with the logic analyzer) or the 100 kOhm Termination Adapters (HP part number 01650-63203).

Figure 4



Connecting the Termination Adapter

To power up or power down

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

To protect the preprocessor interface when not in use

1 Cover the socket assembly pins of the preprocessor interface with a conductive foam wafer or conductive plastic pin protector.

The socket assembly pins of the preprocessor interface were covered at the time of shipment with either a conductive foam wafer or conductive pin protector. If this device is not damaged, it may be reused repeatedly.

2 Store the preprocessor interface in an antistatic bag or container.

Electrostatic Discharge

The socket assembly pins of the preprocessor interface should be covered with a conductive foam wafer or pin protector to protect the delicate gold plated pins of the assembly from damage due to impact. Covering the pins and properly storing the preprocessor interface also protects the active circuitry on the preprocessor interface from electrostatic discharge.

Setting Up the Preprocessor Interface Software

Setting up for the preprocessor interface software consists of the following major steps:

1. **The first time you set up the preprocessor interface, make a duplicate copy of the master disk.**

   For information on duplicating disks, refer to the reference manual for your logic analyzer.

2. **Insert the preprocessor interface disk in the front disk drive of the logic analyzer.**
3. **Load the appropriate configuration file into the logic analyzer.**

   Once you have the hardware and software set up, you are ready to make measurements with the logic analyzer and preprocessor interface. The rest of this section provides more detailed information on setting up the preprocessor software.

To load the configuration and inverse assembler files

1. **Insert the preprocessor interface disk in the front disk drive of the logic analyzer.**
2. **Depending on your logic analyzer, select one of the following menus:**

- For the HP 1650-series logic analyzers, press the I/O menu key and use the knob to select "Disc Operations"
- For the HP 1660-series logic analyzers, select the "System Disk" menu
- For the HP 16500A mainframe, select the "System Front Disk" menu
- For the HP 16500B mainframe, select the "System Flexible Disk" menu

3. **Configure the menu to "Load" the analyzer configuration from disk.**
4. **For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.**
5. **Use the knob to select the appropriate configuration file.**

   Your configuration file choice depends on which analyzer you are using, the software version(s) of your analyzer software, and, in some cases, which inverse assembler you want to use. See the summary table following these instruction steps.

6. **Execute the load operation to load the file into the logic analyzer.**

   The logic analyzer is configured for MC68306 analysis by loading the appropriate MC68306 configuration file. Loading this file also automatically loads the inverse assembler.

   The following table lists the correct configuration file to for each logic analyzer. For more information about the inverse assembler, see Chapter 2.

Table 2 **Logic Analyzer Configuration Files**

Logic Analyzer	Configuration File
1650A/B	C68306E0
1652B	C68306E0
16510A/B	C68306E0
16511B	C68306E2
16550A (one card)	C68306S1
16550A (two card)	C68306S2
16555A (one card)	C68306M1
16555A (two card)	C68306M2
1660A/AS	C68306J0
1661A/AS	C68306S1
1662A/AS	C68306J2

To set up the preprocessor interface for timing

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1 Select the Configuration menu of the logic analyzer.

2 Select the Type field for the analyzer and select Timing.

Analyzing the Motorola MC68306

Analyzing the Motorola MC68306

This chapter describes how to display configuration information and preprocessor interface data, gives status information label and symbol encodings, and provides information about the available inverse assembler.

Displaying Information

This section describes how to display analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

Unwanted Triggers

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most one word, one technique to avoid unwanted triggering from unused prefetches is to add "2" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

To display the format specification

- **Select the format specification menu for your logic analyzer.**

The MC68306 configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessor and any coprocessors connected directly to the microprocessor.

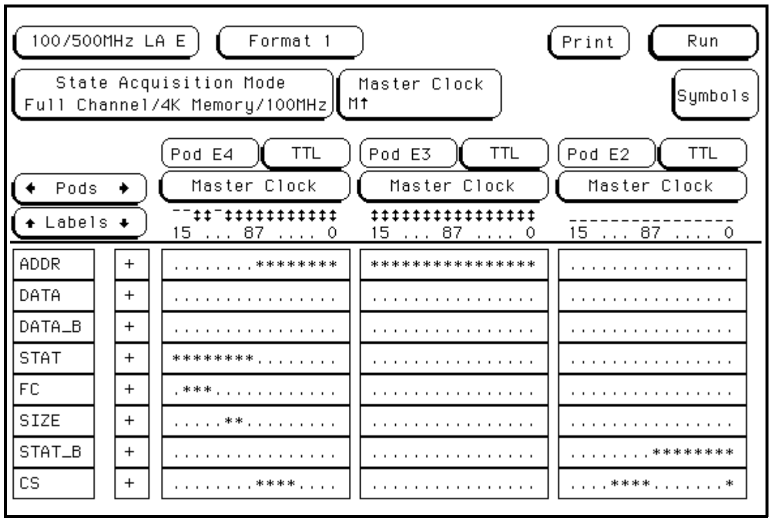
Chapter 3 of this guide contains a table that lists the signals for the MC68306 processor and on which pod and probe line the signal comes to the logic analyzer. Refer to this table and to the logic analyzer connection information for your analyzer in chapter 1 to determine where the processor signals should be on the format specification screen.

> For those logic analyzers which have a Clock Period field, the Clock Period field should remain in the current selection (> 60 ns) to use time-tags. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Example

The format specification display shown in the following figure is from the HP 16550A logic analyzer. Additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

Figure 5



To display the configuration labels and symbols

- **Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.**

The HP E2456A configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific MC68306 cycles easier. The label base in the symbols menu is set to hexadecimal to convserve space in the listing menu.

Table 3

MC68306 STAT Label Bits

Bit	Status Signal	Description
0	R/~W	This signal is high for read cycles and low for write cycles.
1 2	~LDS ~UDS	These active-low signals are the lower and upper data strobes for data bus control.
3	~RESET	If asserted externally, this signal resets the microprocessor. When asserted internally, all external system devices are reset without affecting the internal state of the processor.
4 5 6	FC0 FC1 FC2	These three signals indicate the type of cycle the microprocessor is executing.
7	~BGACK	For 3-wire bus arbitration, this signal is low when the microprocessor has given ownership of the bus to another device. In a 2-wire bus arbitration system, this signal is always high.

Table 4

MC68306 Symbols

Label	Symbol	Pattern (binary)	Description
STAT	dma	0xxx xxxx	direct memory access
	udat wr	1001 xxx0	user data write
	udat rd	1001 xxx1	user data read
	upgm rd	1010 xxx1	user program read
	sdat wr	1101 xxx0	supervisor data write
	sdat rd	1101 xxx1	supervisor data read
	spgm rd	1110 xxx1	supervisor program read
	int ack	1111 xxxx	interrupt acknowledge
	pgm rd	1x10 xxx1	program read
	wr	xxxx xxx0	write
	rd	xxxx xxx1	read
FC	res 0	000	reserved, undefined
	udat 1	001	user data
	upgm 2	010	user program
	res 3	011	reserved, undefined
	res 4	100	reserved, undefined
	sdat 5	101	supervisor data
	spgm 6	110	supervisor program
	cpu 7	111	CPU space
	usr	0xx	user
	sup	1xx	supervisor
	dat	x01	data
	pgm	x10	program
SIZE	word	00	word transfer
	high byte	01	high byte transfer
	low byte	10	low byte transfer
R/~W	rd	1	read
	wr	0	write
DATA_B	BSR	0110 0001 xxxx xxxx	branch to subroutine
	BRA	0110 0000 xxxx xxxx	branch always
	Bxx	0110 xxxx xxxx xxxx	branch
	RTx	0100 1110 0111 0xxx	return
	JSR	0100 1110 10xx xxxx	jump to subroutine
	JMP	0100 1110 11xx xxxx	jump
	Jxx	0100 1110 1xxx xxxx	jump (JMP or JSR)
	---	xxxx xxxx xxxx xxxx	

,

Table 4

MC68306 Symbols

Label	Symbol	Pattern (binary)	Description
CS	cs0	xxxx xxx0 x	signals ~CS3 to ~CS0 are always available
	cs1	xxxx xx0x x	
	cs2	xxxx x0xx x	
	cs3	xxxx 0xxx x	
	cs4	xxx0 xxxx 1	signals ~CS7 to ~CS4 are only available in chip select mode (AMODE=1)
	cs5	xx0x xxxx 1	
	cs6	x0xx xxxx 1	
	cs7	0xxx xxxx 1	
	---	xxxx xxxx x	
BUS	br_bg_ack	000	
	br_bg	001	
	br_ack	010	
	br	011	bus request
	bg_ack	100	
	bg	101	bus grant
	ack	110	bus grant acknowledge
	local	111	MC68306 is bus master

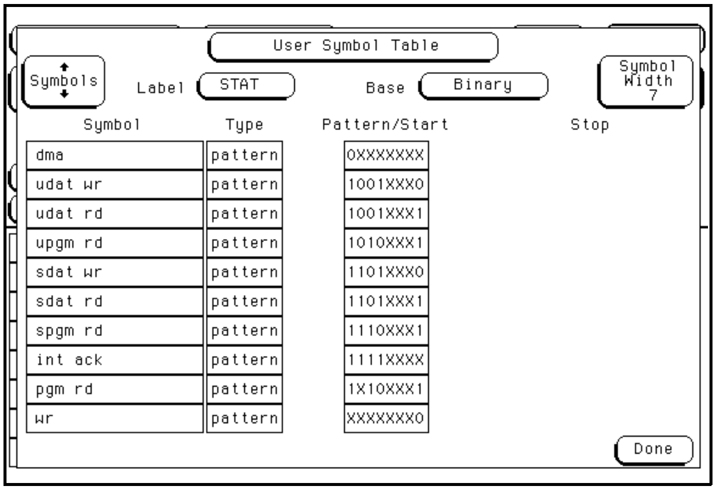
Do not modify the bits in the STAT or DATA labels, or the *lower bits* in the ADDR label in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trigger specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

The lower ADDR bits are bits 0 to 15. You can modify ADDR bits 16 to 23 with no side effects.

Example

The following figure shows the the symbols for the STAT label as displayed by the HP 16550A logic analyzer:

Figure 6



To display captured state data

- **Select the Listing Menu for your logic analyzer.**

The logic analyzer displays captured data in the Listing Menu. The inverse assembler disassembles the captured data in a format that closely resembles the assembly source code for your processor. For those preprocessors that have more than one inverse assembler, the inverse assembler used depends on your logic analyzer and logic analyzer software version. See the logic analyzer software compatibility table in chapter 1.

The inverse assembler often cannot determine where an instruction starts. For correct inverse assembly, you must synchronize the inverse assembler with the start of an instruction. See "To synchronize the inverse assembler" later in this chapter.

If your trace listing doesn't otherwise appear to be correct (capturing the same RAM address twice, for example), make sure the preprocessor interface hardware is configured for state analysis. The "Invasm" field will appear at the top of the Listing Menu screen when the logic analyzer is configured for state analysis. See Chapter 1 to review the hardware configuration, correct it if needed, and then run the trace again.

Example

The following figure shows the Listing Menu display for the HP 16550A logic analyzer using the IA68306 inverse assembler:

Figure 7

Top line of display. Synchronization begins here.

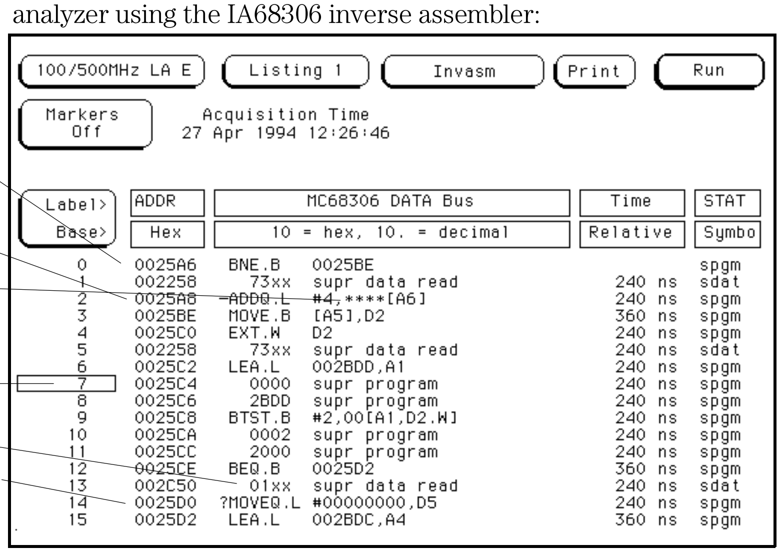
Unexecuted prefetch

Missing opcodes (caused by unexecuted prefetch)

Cursor position

Don't care bytes

Prefetch that may or may not have been executed.



Using the Inverse Assembler

This section discusses the general output format of the inverse assembler, and any processor-specific information you will need.

The MC68306 microprocessor does not indicate externally which word fetched is the beginning of a new instruction. You may have to "point" to the first state of an instruction fetch to synchronize the inverse assembler. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen. See "To synchronize the inverse assembler" later in this chapter for more information.

General Output Format

The next few paragraphs describe the general output format of the inverse assembler.

Numeric Format

Unless a value is followed by a suffix character, numeric output from the inverse assembler is in hexadecimal format. For example, decimal values have a period (.) as the suffix character; binary values have a percent sign (%).

Missing Opcodes

Asterisks (*) in the inverse assembler output indicate that a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

Don’t Care Bytes

The MC68306 microprocessor can perform byte, word, and long word transfers. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. lines. The inverse assembler displays "xx" for any bytes in a transfer that are ignored by the microprocessor. You can determine exactly which byte or bytes of data were used as an operand.

Unexecuted Prefetched Instructions

The preprocessor interface sends all of the bus transactions by both the microprocessor and coprocessor to the logic analyzer. Prefetched instructions which are not executed by the microprocessor are marked by a hyphen "-".

In some cases, it is impossible to determine from bus activity whether a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?".

IA68306 Processor-Specific Output Format

This section discusses issues specific to the IA68306 inverse assembler.

Bus Arbitration

Use of two-wire bus arbitration may cause the inverse assembler to incorrectly disassemble state information. See the "Theory of Operation and Clocking" section in Chapter 3 for more information.

PC-based Addressing Modes

The microprocessor may occasionally make an operand fetch from program space when program-counter-based (PC-based) addressing modes are used.

```
MOVE.L  0[PC,D0.L],D7
```

When this occurs, the resulting memory read is classified as a program reference by the microprocessor, and the Function Code lines are driven accordingly (they indicate a program read rather than a data read).

When the inverse assembler detects an instruction of this type, it will attempt to locate the operand fetch and tag it so that it will not be disassembled. Instead, it will be classified as "program data" by the inverse assembler and displayed in hexadecimal format.

In the following example, state 350 has the instruction, and states 355 and 356 have the data.

Label	> ADDR	DATA		STAT
Base	> Hex	Invasm		Symbol
348	04D214	MOVE.L	D7,FFCE[A4]	upgm rd
349	04D216	FFCE	user program read	upgm rd
350	04D218	MOVE.L	04D654[PC],-[A7]	upgm rd
351	F4083E	43D8	user data write	udat rd
352	F40840	6DFB	user data write	udat rd
353	F4D21A	043A	user program read	upgm rd
354	04D21C	MOVE.L	D7,-[A7]	upgm rd
355	04D654	4400	user program data	upgm rd
356	04D656	0000	user program data	upgm rd
357	04D21E	JSR	03523C	upgm rd
358	086BBC	0000	user data write	udat rd
359	086BBA	4400	user data write	udat rd
360	04D220	0003	user program read	upgm rd
361	086BB8	6DFB	user data write	udat rd
362	086BB6	43D8	user data write	udat rd
363	04D222	523C	user program read	upgm rd

PC-based Addressing Mode Listing

To synchronize the inverse assembler

1 **Identify a line on the display that you know is the first state of an instruction fetch.**

2 **Roll this line to the top of the listing.**

3 **Select the "Invasm" field at the top of the screen.**

The listing will inverse assemble from the top line down. Any data before this screen is left unchanged. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the listing by entering a new line number or by rolling the screen down, you may have to re-synchronize the inverse assembler by repeating the described steps.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

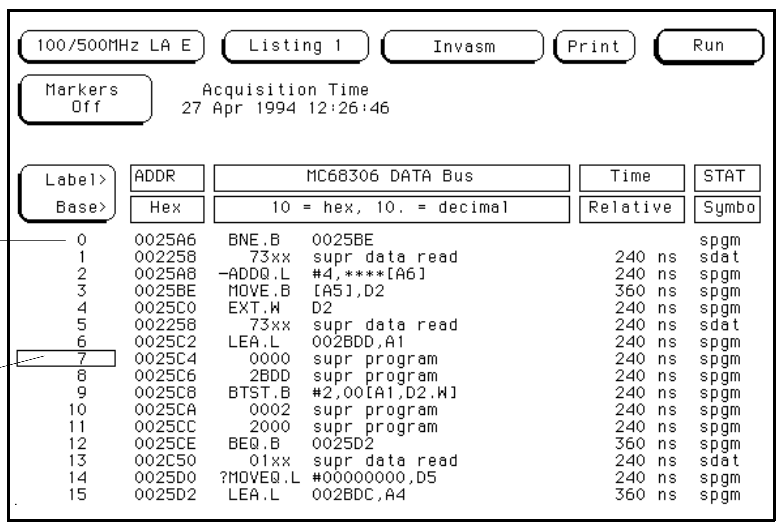
Example

Synchronize the inverse assembler by positioning the first instruction to be disassembled at the top of the listing display and choosing "Invasm" from the top of the display.

Figure 8

Synchronization begins at the top of the display, not at the cursor position.

Cursor position.



Inverse Assembler Error Messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request

Displayed if the inverse assembler is used with an instrument other than the supported logic analyzers.

Fatal Data Error

Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Invalid Status

Displayed if the status field for the current state is not valid.

Illegal Opcode

Displayed if the inverse assembler encounters an illegal instruction.

Reserved Opcode

Displayed if the inverse assembler encounters a reserved coprocessor instruction.

No Operand

Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP E2456A hardware including the characteristics and signal mapping for the preprocessor interface. This chapter also includes a brief theory of operation, circuit board dimensions, and information on repairing the preprocessor interface.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Table 5 **Operating Characteristics**

Microprocessor Compatibility	Motorola MC68306 microprocessor	
Microprocessor Package	132-pin QFP	
	The HP E2456A does not support the 144-pin TQFP processor package.	
Accessories Required	HP E3417A generic PGA to 132-pin QFP probe adapter.	
Maximum Clock Speed	16.67 MHz Clockout (8.33 MHz ~AS rate).	
Power Requirements	100 mA at +5 Vdc maximum, supplied by the logic analyzer.	
Probes Required	Seven 16-channel pods are available. Three are required for inverse assembly with state analysis.	
Signal Line Loading	Loading when using only pods P1, P3, and P4 is 20 pF in parallel with 100 kOhm on all lines (except 10 pF on EXTAL and XTAL). Connecting additional pods may increase loading on certain signals.	
Environmental Temperature	Operating Nonoperating	0 to 55 degrees C (+32 to +131 degrees F) -40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating Nonoperating	4,600 m (15,000 ft) 15,300 m (50,000 ft)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Theory of Operation and Clocking

Clocking

The microprocessor address strobe (~AS) indicates that address, function code, size, and R/~W state information is on the bus and valid. The rising edge of ~AS is used to clock information into the logic analyzer.

On a read cycle, data must be valid for 10 ns before the rising edge of ~AS for all logic analyzers except the HP 1660A/61A/62A, HP 16550A, and HP 16555A.

Bus Arbitration

Bus arbitration is the method used by the microprocessor and other possible bus master devices to request, grant, and acknowledge bus ownership. The MC68306 microprocessor provides two different ways to arbitrate the bus, 2-wire and 3-wire arbitration.

If 3-wire bus arbitration is used, the ~BGACK signal is asserted when the microprocessor has given ownership of the bus to another device. The inverse assembler will not attempt to interpret any data as instruction fetches until ~BGACK is negated.

In 2-wire bus arbitration, however, ~BGACK must always be pulled high. Signals ~BR and ~BG indicate changes in bus control, but are asynchronous with ~AS which clocks the logic analyzer. The inverse assembler has no way of positively determining whether the microprocessor has bus control and instead must rely on the function code signals. Once another device assumes bus ownership, the microprocessor tri-states the function code lines. If the new bus master happens to drive the function codes to combinations which are recognized as valid by the inverse assembler, then incorrect disassembly may result.

If your microprocessor target system uses 2-wire bus arbitration, you can work around this potential problem by synchronizing the inverse assembler on the first state of an instruction fetch which occurs at least one or more states after ~BG goes high.

Signal-to-Connector Mapping

The following figure shows the pin numbers and microprocessor signals for the preprocessor interface pin-grid-array socket.

	1	2	3	4	5	6	7	8	9	10	11	12
A	50 N/C	51 FC1	54 ~BERR	57 D14	61 VDD	65 D7	69 D4	73 VDD	76 IRQ4	80 ~IACK4	82 PB7	83 N/C
B	49 FC2	48 ~RESET	52 FC0	58 D13	62 D10	66 D6	68 D5	72 D1	78 ~IACK7	79 GND	81 ~IACK1	84 PB6
C	47 ~HALT	46 GND	53 ~DTACK	55 GND	59 D12	63 D9	71 D2	75 IRQ7	77 IRQ1	86 PB4	85 PB5	87 PB3
D	43 EXTAL	45 CLKOUT	44 XTAL	56 D15	60 D11	64 D8	70 D3	74 D0	89 PB2	88 GND	91 PB0	90 PB1
E	40 VDD	39 ~BGACK	42 ~BR	41 ~BG	GP7 GND	GP8 GND	67 GND	GP6 GND	93 PA6	92 PA7	95 PA5	94 VDD
F	36 ~UDS	35 ~LDS	38 ~AS	37 R/~W	34 GND	GP9 GND	GP4 GND	GP5 GND	97 PA3	96 PA4	99 PA1	98 PA2
G	32 ~LW	33 ~UW	30 ~DRAMW	31 ~OE	GPB GND	GPA GND	GP3 GND	100 GND	103 X2	104 IP2	101 PA0	102 X1
H	28 VDD	29 ~RAS1	26 ~CAS1	27 ~RAS0	GPC GND	1 GND	GP2 GND	GP1 GND	107 RXDA	108 TXDA	105 OP3	106 VDD
J	24 ~CS0	25 ~CAS0	22 GND	23 ~CS1	8 A6	4 A9	130 A14	126 A17	122 TDO	110 TXDB	111 IP0	109 RXDB
K	21 ~CS2	19 A20	20 ~CS3	11 A3	9 A5	5 A8	129 A15	125 A18	121 GND	119 TMS	112 GND	113 IP1
L	18 A21	15 A23	13 GND	12 A2	6 A7	2 A11	132 A12	128 A16	124 A19	118 TCK	114 OP0	115 OP1
M	17 N/C	16 A22	14 A1	10 A4	7 VDD	3 A10	131 A13	127 VDD	123 AMODE	120 TDI	117 ~TRST	116 N/C

Notation: ~ indicates signal is active low.

PGA Pin Assignments

The following table describes the electrical interconnections implemented with the preprocessor interface.

The signal list table column descriptions are as follows:

POD	The preprocessor connector that carries the signal.
PIN	The probe within the pod that carries the signal.
LA BIT	The logic analyzer bit associated with the signal.
PGA PIN	The PGA adapter pin associated with the signal.
QFP PIN	The microprocessor package pin number.
68306 LABEL	The manufacturer's signal name.
BUS LABEL	An analyzer bus label identifies a collection of signals, such as all ADDR or DATA. This signal is one of those in the bus label.
ALT BUS	An additional bus label also assigned to the signal (if any).
SIG LABEL	An individual analyzer label associated with this signal only.

Table 6

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P1[1]	19	0	D8	74	D0	DATA		
P1[1]	18	1	B8	72	D1	DATA		
P1[1]	17	2	C7	71	D2	DATA		
P1[1]	16	3	D7	70	D3	DATA		
P1[1]	15	4	A7	69	D4	DATA		
P1[1]	14	5	B7	68	D5	DATA		
P1[1]	13	6	B6	66	D6	DATA		
P1[1]	12	7	A6	65	D7	DATA		
P1[1]	11	8	D6	64	D8	DATA		
P1[1]	10	9	C6	63	D9	DATA		
P1[1]	9	10	B5	62	D10	DATA		
P1[1]	8	11	D5	60	D11	DATA		
P1[1]	7	12	C5	59	D12	DATA		
P1[1]	6	13	B4	58	D13	DATA		
P1[1]	5	14	A4	57	D14	DATA		
P1[1]	4	15	D4	56	D15	DATA		
P1	3	Clock 1	C3	53	~DTACK			~DTACK (J clock)

Notation:

~ Signal is active low.

1 Signal is required for inverse assembly.

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P2	19	0	M9	123	AMODE	STAT_B		AMODE
P2	18	1	C3	53	~DTACK	STAT_B		~DTACK
P2	17	2	G4	31	~OE	STAT_B		~OE
P2	16	3	G1	32	~LW	STAT_B		~LW
P2	15	4	G2	33	~UW	STAT_B		~UW
P2	14	5	C1	47	~HALT	STAT_B		~HALT
P2	13	6	A3	54	~BERR	STAT_B		~BERR
P2	12	7	F3	38	~AS	STAT_B		~AS
P2	11	8	J1	24	~CS0	CS		~CS0
P2	10	9	J4	23	~CS1	CS		~CS1
P2	9	10	K1	21	~CS2	CS		~CS2
P2	8	11	K3	20	~CS3	CS		~CS3
P2[5]	7	12	E2	39	~BGACK	BUS		
P2	6	13	E4	41	~BG	BUS		~BG
P2	5	14	E3	42	~BR	BUS		~BR
P2	4	15	D2	45	CLKOUT			CLKOUT
P2	3	Clock 1	L10	118	TCK			TCK (K clock)

Notation:

~ Signal is active low.

5. Although ~BGACK is available on both preprocessor connectors P2 and P4, the individual signal label is assigned to P4 in the logic analyzer Format menu because this pod connection is required for inverse assembly. The P2 version of ~BGACK is used as one of the bits for BUS LABEL "BUS".

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P3[1,2]	19	0	F1	36	~UDS	ADDR		
P3[1]	18	1	M3	14	A1	ADDR		
P3[1]	17	2	L4	12	A2	ADDR		
P3[1]	16	3	K4	11	A3	ADDR		
P3[1]	15	4	M4	10	A4	ADDR		
P3[1]	14	5	K5	9	A5	ADDR		
P3[1]	13	6	J5	8	A6	ADDR		
P3[1]	12	7	L5	6	A7	ADDR		
P3[1]	11	8	K6	5	A8	ADDR		
P3[1]	10	9	J6	4	A9	ADDR		
P3[1]	9	10	M6	3	A10	ADDR		
P3[1]	8	11	L6	2	A11	ADDR		
P3[1]	7	12	L7	132	A12	ADDR		
P3[1]	6	13	M7	131	A13	ADDR		
P3[1]	5	14	J7	130	A14	ADDR		
P3[1]	4	15	K7	129	A15	ADDR		
P3	3	Clock 1	D2	45	CLKOUT			CLKOUT (L clock)

Notation:

~ Signal is active low.

1 Signal is required for inverse assembly.

2 This is a delayed version of the signal (10 nsec) for state analysis.

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P4[1]	37	0	L8	128	A16	ADDR		
P4[1]	35	1	J8	126	A17	ADDR		
P4[1]	33	2	K8	125	A18	ADDR		
P4[1]	31	3	L9	124	A19	ADDR		
P4[1]	29	4	K2	19	A20	ADDR	CS	~CS4
P4[1]	27	5	L1	18	A21	ADDR	CS	~CS5
P4[1]	25	6	M2	16	A22	ADDR	CS	~CS6
P4[1]	23	7	L2	15	A23	ADDR	CS	~CS7
P4[1]	21	8	F4	37	R/~W	STAT		R/~W
P4[1,2]	19	9	F2	35	~LDS	STAT	SIZE	~LDS
P4[1,2]	17	10	F1	36	~UDS	STAT	SIZE	~UDS
P4	15	11	B2	48	~RESET	STAT		~RESET
P4[1]	13	12	B3	52	FC0	STAT	FC	FC0
P4[1]	11	13	A2	51	FC1	STAT	FC	FC1
P4[1]	9	14	B1	49	FC2	STAT	FC	FC2
P4[1,5]	7	15	E2	39	~BGACK	STAT		~BGACK
P4[1]	3	Clock 1	F3	38	~AS			~AS (M clock)

Notation:

~ Signal is active low.

1 Signal is required for inverse assembly.

2 This is a delayed version of the signal (10 nsec) for state analysis.

5. Although ~BGACK is available on both preprocessor connectors P2 and P4, the individual signal label is assigned to P4 in the logic analyzer Format menu because this pod connection is required for inverse assembly. The P2 version of ~BGACK is used as one of the bits for BUS LABEL "BUS".

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P5	19	0	J2	25	~CAS0	DRAM		~CAS0
P5	18	1	H3	26	~CAS1	DRAM		~CAS1
P5	17	2	H4	27	~RAS0	DRAM		~RAS0
P5	16	3	H2	29	~RAS1	DRAM		~RAS1
P5	15	4	G3	30	~DRAMW	DRAM		~DRAMW
P5	14	5	B11	81	~IACK1	INT		~IACK1
P5	13	6	A10	80	~IACK4	INT		~IACK4
P5	12	7	B9	78	~IACK7	INT		~IACK7
P5	11	8	C9	77	IRQ1	INT		IRQ1
P5	10	9	A9	76	IRQ4	INT		IRQ4
P5	9	10	C8	75	IRQ7	INT		IRQ7
P5	8	11	M11	117	~TRST	JTAG		~TRST
P5	7	12	J9	122	TDO	JTAG		TDO
P5	6	13	M10	120	TDI	JTAG		TDI
P5	5	14	K10	119	TMS	JTAG		TMS
P5	4	15	L10	118	TCK	JTAG		TCK
P5[4]	3	Clock 1			N/C			

Notation:

~ Signal is active low.

4. "No Connect." Signal is not passed through to the logic analyzer.

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P6	19	0	D11	91	PB0	PORT_B		~IACK2
P6	18	1	D12	90	PB1	PORT_B		~IACK3
P6	17	2	D9	89	PB2	PORT_B		~IACK5
P6	16	3	C12	87	PB3	PORT_B		~IACK6
P6	15	4	C10	86	PB4	PORT_B		IRQ2
P6	14	5	C11	85	PB5	PORT_B		IRQ3
P6	13	6	B12	84	PB6	PORT_B		IRQ5
P6	12	7	A11	82	PB7	PORT_B		IRQ6
P6	11	8	G11	101	PA0	PORT_A		
P6	10	9	F11	99	PA1	PORT_A		
P6	9	10	F12	98	PA2	PORT_A		
P6	8	11	F9	97	PA3	PORT_A		
P6	7	12	F10	96	PA4	PORT_A		
P6	6	13	E11	95	PA5	PORT_A		
P6	5	14	E9	93	PA6	PORT_A		
P6	4	15	E10	92	PA7	PORT_A		
P6[4]	3	Clock 1			N/C			

Notation:

~ Signal is active low.

4. "No Connect." Signal is not passed through to the logic analyzer.

Table 6 (Cont.)

MC68306 Signal List

POD	PIN	LA BIT	PGA PIN	QFP PIN	68306 LABEL	BUS LABEL	ALT BUS	SIG LABEL
P7[3]	19	0	F2	35	~LDS			~LDS_T
P7[3]	18	1	F1	36	~UDS			~UDS_T
P7[4]	17	2			N/C			
P7[4]	16	3			N/C			
P7	15	4	J11	111	IP0	SERIAL		IP0
P7	14	5	K12	113	IP1	SERIAL		IP1
P7	13	6	G10	104	IP2	SERIAL		IP2
P7	12	7	L11	114	OP0	SERIAL		OP0
P7	11	8	L12	115	OP1	SERIAL		OP1
P7	10	9	H11	105	OP3	SERIAL		OP3
P7	9	10	J10	110	TXDB	SERIAL		TXDB
P7	8	11	J12	109	RXDB	SERIAL		RXDB
P7	7	12	H10	108	TXDA	SERIAL		TXDA
P7	6	13	H9	107	RXDA	SERIAL		RXDA
P7	5	14	G12	102	X1	SERIAL		X1
P7	4	15	G9	103	X2	SERIAL		X2
P7	3	Clock 1			N/C			

Notation:

~ Signal is active low.

3. This is an undelayed version of the signal for timing analysis.

4. "No Connect." Signal is not passed through to the logic analyzer.

MC68306 Power/Ground Mapping

Although the VDD pins for the microprocessor are brought out to the preprocessor PGA socket, the preprocessor interface does not use the microprocessor's power; these pins are treated as no-connects. The "Shield" signal below is connected to the preprocessor interface ground but does not correspond to any particular MC68306 GND pin.

Table 7 **MC68306 Power/Ground List**

HP E2456A PGA Pin	MC68306 QFP-132 Pin	MC68306 Signal Name
H6	1	GROUND
M5	7	VDD
L3	13	GROUND
J3	22	GROUND
H1	28	VDD
F5	34	GROUND
E1	40	VDD
C2	46	GROUND
C4	55	GROUND
A5	61	VDD
E7	67	GROUND
A8	73	VDD
B10	79	GROUND
D10	88	GROUND
E12	94	VDD
G8	100	GROUND
H12	106	VDD
K11	112	GROUND
K9	121	GROUND
M8	127	VDD
E5	N/C	Shield
E6	N/C	Shield
E8	N/C	Shield
F6	N/C	Shield
F7	N/C	Shield
F8	N/C	Shield

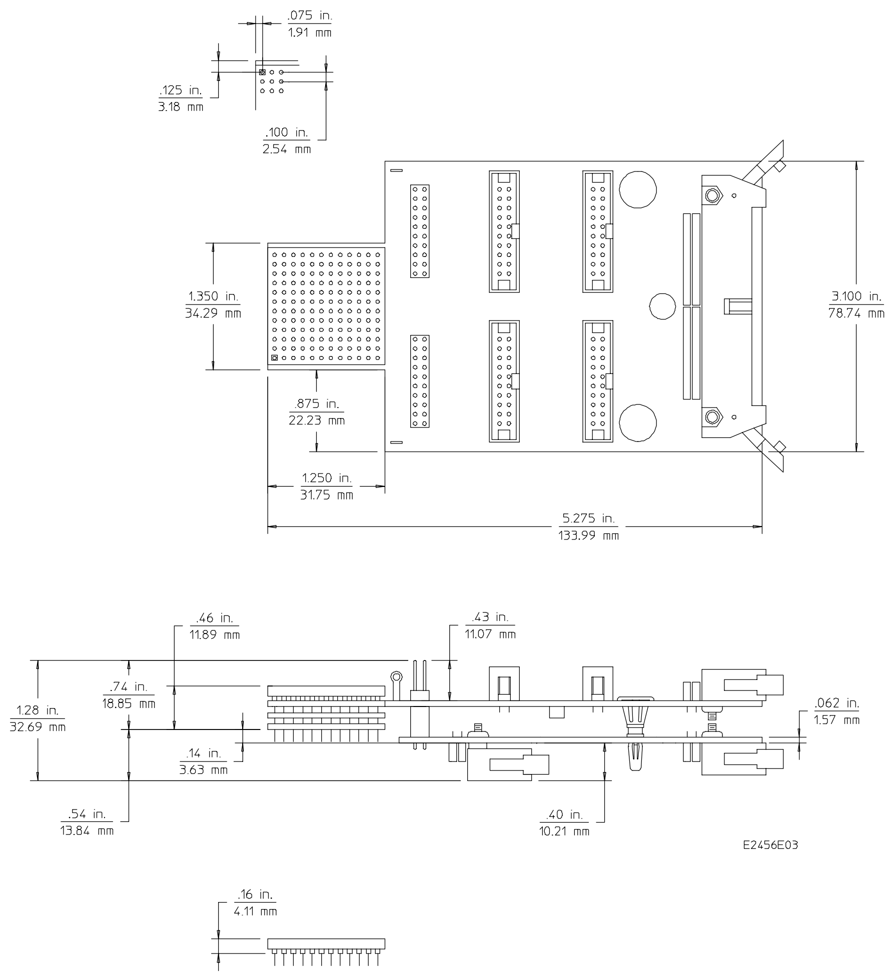
Table 7 **MC68306 Power/Ground List**

HP E2456A PGA Pin	MC68306 QFP-132 Pin	MC68306 Signal Name
G5	N/C	Shield
G6	N/C	Shield
G7	N/C	Shield
H5	N/C	Shield
H7	N/C	Shield
H8	N/C	Shield

Circuit Board Dimensions

Figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.

Figure 9



Dimensions

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 8 **Replaceable Parts**

HP Part Number	Description
HP E2456-66501	Identity circuit board assembly (upper)
HP E2413-66505	ADDR/DATA circuit board assembly (lower)
HP E2456-68701	Inverse assembler disk pouch
5081-7736	Generic PGA to 132-pin QFP probe adapter
1200-1712	PGA pin protector socket

A

If You Have a Problem

If You Have a Problem

Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

If you still have difficulty using the analyzer after trying the suggestions in this chapter, please contact your local Hewlett-Packard service center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and preprocessors. Otherwise, you may damage circuitry in the analyzer, preprocessor, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

☐ **Remove and reseat all cables and probes; ensure that there are no bent pins on the preprocessor interface or poor probe connections.**

☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**

☐ **Use an oscilloscope to check the signal integrity of the data lines.**

Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also

See “Capacitive Loading” in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most one word, one technique to avoid unwanted triggering from unused prefetches is to add "2" to the trigger address. The trigger condition will only be satisfied if the branch is not taken.

No activity on activity indicators

- ☐ On the HP 16510A Logic Analyzer, check the fuse that allows power to the preprocessor interface.
- ☐ On other logic analyzers, check for loose cables, board connections, and preprocessor interface connections.
- ☐ Check for bent or damaged pins on the preprocessor probe.

No trace list display

If there is no trace list display, it may be that your analysis specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your analysis sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Preprocessor Problems

This section lists problems that you might encounter when using a preprocessor. If the solutions suggested here do not correct the problem, you may have a defective preprocessor. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the preprocessor interface, the microprocessor (if socketed) or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- ☐ Ensure that you are following the correct power-on sequence for the preprocessor and target system.

  1. Power up the analyzer and preprocessor.
  2. Power up the target system.

  If you power up the target system before you power up the preprocessor, interface circuitry in the preprocessor may latch up, preventing proper target system operation.

- ☐ Verify that the microprocessor and the preprocessor interface are properly rotated and aligned, so that the index pin on the microprocessor (such as pin 1 or A1) matches the index pin on the preprocessor interface.

- ☐ Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.

- ☐ Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and are firmly inserted.

- ☐ Reduce the number of extender sockets.

See Also "Capacitive Loading" in this appendix.

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Ensure that the preprocessor configuration switches are correctly set for the measurement you are trying to make.**

  Some preprocessors include configuration switches for various features (for example, to allow dequeueing of the trace list). See chapter 1 for information about setting configuration switches.

- ☐ **Try doing a full reset of the target system before beginning the measurement.**

  Some preprocessor designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the preprocessor probe installed.**

  See "Capacitive Loading" in this chapter. While preprocessor loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning, giving erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Microprocessors such as the i486, Pentium™, and MC68040 generate substantial heat. This is exacerbated by the active circuitry on the preprocessor board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the preprocessor interface, or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ Remove as many pin protectors, extenders, and adapters as possible.
- ☐ If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the preprocessor or in your target system. If you follow the suggestions in this section to ensure that you are using the preprocessor and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem is due to incorrect synchronization, modified configuration, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

☐ **Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the cursor position) and pressing the Invasm key.**

Because the inverse assembler works from the first line of the trace *display*, if you jump to the middle of a trace and select Invasm, prior trace states may not be disassembled correctly. If you move to several random places in the trace list and synchronize the disassembly each time, the trace disassembly is only guaranteed to be correct for the portion of the trace list disassembled. See "To synchronize the inverse assembler" in Chapter 2 for more information.

☐ **Ensure that each logic analyzer pod is connected to the correct preprocessor connector.**

There is not always a one-to-one correspondence between analyzer pod numbers and preprocessor cable numbers. Preprocessors must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order, so the cable connections for each preprocessor are often altered to support that need. Thus, one preprocessor might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See chapter 1 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some preprocessors also require other data labels; see chapter 2 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **Ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler or rename it, the configuration process will fail to load the disassembler.

  See chapter 1 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed, due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer, because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

☐ **Adjust the skew in the Intermodule menu.**

You may be able to specify a skew value that enables the event to be captured.

☐ **Change the trigger specification for modules upstream of the one with the problem.**

If you're using a logic analyzer to trigger the scope, try specifying a trigger state one state before the one you are using. This may be more difficult than working with the skew, because the prior state may occur more often and not always be related to the event you're trying to capture with the oscilloscope.

Messages

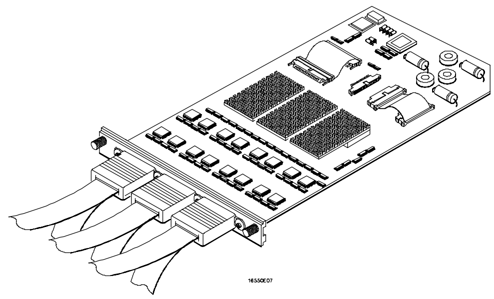
This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Inverse Assembler Not Found"

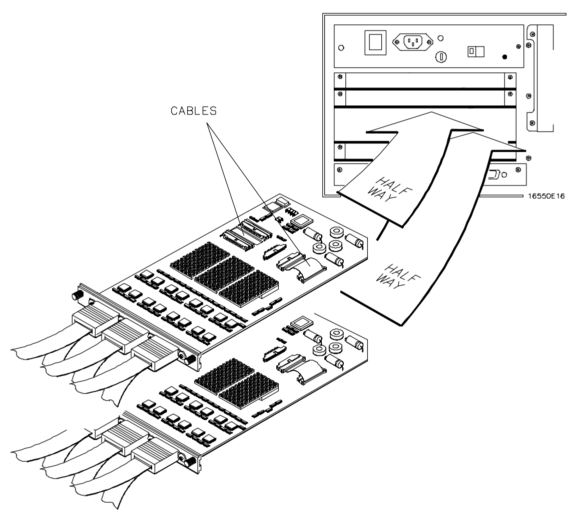
This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

“Measurement Initialization Error”

This error occurs when you have installed the cables incorrectly for one or two HP 16550A logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card installations. Ensure that your cable connections match the drawing, then repeat the measurement.



Cable Connections for One-Card HP 16550A Installations



Cable Connections for Two-Card HP 16550A Installations

See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

“No Configuration File Loaded”

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

See Also Chapter 1 describes how to load configuration files.

“Selected File is Incompatible”

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

“Slow or Missing Clock”

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/B or HP 16501A frame. Ensure that the cards are firmly seated.

- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.

- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the preprocessor interface. See chapter 1 to determine the proper connections.

- ☐ For HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

> The error message "State Clock Violates Overdrive Specification" should occur only for HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to <60 ns. If this error message is observed with the Clock Period set to >60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales Office for information on servicing the instrument.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- ☐ **When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.**

If a "don't care" trigger condition is set, this message indicates:

- ☐ For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."

- ☐ For an HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trigger correctly for the measurement that is desired.

DECLARATION OF CONFORMITY

according to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name:	Hewlett-Packard Company
Manufacturer's Address:	1900 Garden of the Gods Road Colorado Springs , CO 80901 U.S.A.

Declares, That the product

Product Name:	Preprocessor Interface
Model Number(s):	HP E2456A
Product Options:	All

Conforms to the following Product Specifications:

Safety:	IEC 348 / HD 401 UL 1244 CSA - C22.2 No. 231 Series M-89
EMC:	CISPR 11:1990 /EN 55011 (1991): Group 1 Class A IEC 801-2:1991 /EN 50082-1 (1992): 4 kV CD, 8 kV AD IEC 801-3:1984 /EN 50082-1 (1992): 3 V/m IEC 801-4:1988 /EN 50082-1 (1992): 1 kV

Supplementary Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC.

Colorado Springs, July 5, 1993

John H. Strathman

John Strathman, Quality Manager

European Contact: Your local Hewlett-Packard Sales and Service Office or Hewlett-Packard GmbH, Department ZQ / Standards Europe, Herrenberger Strasse 130, 71034 Böblingen Germany (FAX: +49-7031-143143)

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Hewlett-Packard
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901

About this edition

This is the first edition of the *HP E2456A MC68306 Preprocessor Interface User's Guide*. Edition dates are as follows:

1st edition, June, 1994

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by you. The dates on the title page change only when a new edition is published.

A software or firmware code may be printed before the date. This code indicates the version level of the software or firmware of this product at the time the manual or update was issued. Many product updates and fixes do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

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June, 1994: All pages original edition